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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,179	03/24/2004	Michael C. Lewis	BP1416/1262C	4584

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SAWYER LAW GROUP LLP
P O BOX 51418
PALO ALTO, CA 94303

EXAMINER	
CASCHERA, ANTONIO A	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,179	LEWIS ET AL.	
	Examiner	Art Unit	
	Antonio A Caschera	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 March 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3/24/04.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. This application filed under former 37 CFR 1.60 lacks the necessary reference to the prior application. A statement reading "This is a continuation of Application No. 09/306,877, filed 05/07/1999." should be entered following the title of the invention or as the first sentence of the specification. Also, the current status of all nonprovisional parent applications referenced should be included.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:

The oath submitted is not directed to the current application no. 10/808,179 but instead is the oath filed for application 09/306,877 from which priority is claimed.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract currently comprises the language of, "A method and system for processing textures for a graphical image on a display is disclosed," (see lines 1-2 of the abstract), which should be corrected.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: #198 mentioned on page 23, 1st paragraph of the specification. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 2, 6, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Watkins (U.S. Patent 5,598,517).

In reference to claims 1 and 8, Watkins discloses a multiple-level scanning approach to scan process primitives (see column 2, lines 44-45). Watkins discloses a system and method for implementing this multiple-level technique comprising a plurality of sets of rendering processors with multi-level scanners each coupled to a texture memory and a frame buffer memory (see column 3, lines 61-62, column 9, lines 10-15 and Figure 8). Watkins specifically discloses the processors operating upon fragments of data of frame buffer and texture memories (see column 9, lines 36-49). Watkins also discloses each of the plurality of processors to operate upon fragment data concurrently, therefore making them operate in parallel (see column 9, lines 25-31). Watkins discloses each processor to operate based upon the process shown in Figure 6, whereby a plurality of portions of data, including texture data, are processed (see column 9, lines 36-49). Note, the office interprets the rendering processors of Watkins to inherently comprise of some sort of memory or register for storing some sort of program, instruction or firmware in accordance with the process shown in Figure 6, since each processor operates in a specific area of the display called panels (see columns 8-9, lines 67-9). Further note, the flow of the process shown in Figure 6, conditions are tested to see if a second, third, fourth etc. portion of data exists (see #74, 78, 82 of Figure 6) and therefore the office interprets the plurality of processors processing a plurality of additional portions of data.

In reference to claims 2 and 9, Watkins discloses all of the claim limitations as applied to claims 1 and 8 respectively above in addition, Watkins discloses a distributor which distributes data to the processors (see column 9, lines 33-36 and #102 of Figure 8). Note, the office

interprets the distributor of Watkins to provide texture data as Watkins discloses the distributor providing data for each panel to the processors (see column 9, lines 33-34).

In reference to claim 6, Watkins discloses all of the claim limitations as applied to claim 1 above. Watkins discloses a system for implementing this multiple-level technique comprising a plurality of sets of rendering processors with multi-level scanners each coupled to a texture memory and a frame buffer memory (see column 3, lines 61-62, column 9, lines 10-15 and Figure 8). Watkins specifically discloses the processors operating upon fragments of data of frame buffer and texture memories (see column 9, lines 36-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3, 7 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,598,517) in view of Yamaguchi et al. (U.S. 6,040,844).

In reference to claim 3, Watkins discloses all of the claim limitations as applied to claim 2 above. Watkins does not explicitly disclose an argument decoder for providing the plurality of texture portions to the distributor and for performing at least one operation on a third portion of the plurality of texture portions. Yamaguchi et al. discloses a method and apparatus for mapping texture data of three-dimensional computer graphics (see column 1, lines 1-13). Yamaguchi et

al. discloses processing texture data in parallel using multiple texture mapping units coupled to a DDA unit (see column 15, lines 41-44, #101a, 102a and 102b of Figure 5). Yamaguchi et al. further discloses the DDA unit to linearly interpolate color values and texture coordinates for a given pixel of a polygon and pass this data onto each texture mapping unit (see column 6, lines 1-8). Note, the office interprets the DDA unit functionally equivalent to applicant's decoder since it performs interpolation of texture coordinates before passing data onto further texture processing. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interpolation in parallel processing techniques of Yamaguchi et al. with the texture parallel processing techniques of Watkins in order to enhance image data processing for picture generation while flexibly mapping texture data at increased speeds and at lower costs (see column 5, lines 4-7 of Yamaguchi et al.).

In reference to claims 7 and 10, Watkins discloses all of the claim limitations as applied to claims 6 and respectively 9 above. Watkins discloses the display to include a plurality of pixels, wherein a plurality of fragments intersect a portion of the plurality of pixels (see column 5, lines 29-30, column 4, lines 18-24 and Figure 1). Watkins does not explicitly disclose the plurality of texture portions as texels. Yamaguchi et al. discloses a method and apparatus for mapping texture data of three-dimensional computer graphics (see column 1, lines 1-13). Yamaguchi et al. discloses processing texture data in parallel using multiple texture mapping units coupled to a DDA unit (see column 15, lines 41-44, #101a, 102a and 102b of Figure 5). Yamaguchi et al. further discloses the DDA unit to linearly interpolate color values and texture coordinates for a given pixel of a polygon and pass this data onto each texture mapping unit (see column 6, lines 1-8). Note, the office interprets the interpolated texture coordinate data of

Yamaguchi et al. functionally equivalent to texel data since this texture data is representative of drawing pixels which in turn represent a portion of the picture for display. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interpolation in parallel processing techniques of Yamaguchi et al. with the texture parallel processing techniques of Watkins in order to enhance image data processing for picture generation while flexibly mapping texture data at increased speeds and at lower costs (see column 5, lines 4-7 of Yamaguchi et al.).

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,598,517).

In reference to claim 4, Watkins discloses all of the claim limitations as applied to claim 1 above however, Watkins does not explicitly disclose the memory further including a cache. At the time the invention was made, it would have been obvious to one of ordinary skill in the art to implement a cache type memory unit in the processors of Watkins since such type of memory is and was, at the time of the invention, commonly found in processors. Applicant has not disclosed that specifically implementing a cache type memory unit provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicant's invention to perform equally well with the processors of Watkins because the exact type of memory unit, in this case, is a matter of design choice as preferred by the designer and to which best suits the application at hand. Therefore, it would have been obvious to one of ordinary skill in this art to modify Watkins to obtain the invention as specified in claim 4.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,598,517) in view of Rentschler et al. (U.S. 5,821,950).

In reference to claim 12, Watkins discloses all of the claim limitations as applied to claim 8 above however, Watkins does not explicitly disclose blending the texture potions in the texture processors according to at least one program. Rentschler et al. discloses methods and apparatus for parallel processing of vertex data in a computer graphics system (see column 2, lines 18-20). Rentschler et al. discloses multiple texture mapping units coupled to multiple 3D geometry accelerators, the texture mapping units operable in a "blending mode" where texture color values are combined and controlled by a rendering mode control word via a bus line (see column 5, lines 44-47, #28 of Figure 1 and #32A-D, 46A and 46B, of Figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the blending mode operations on texture data of Rentschler et al. with the parallel processing of texture data of Watkins in order to combine data of parallel processors more efficiently creating enhanced parallel processing performance in a computer graphics system (see column 1, lines 7-10 and column 2, line 3-16 of Rentschler et al.).

9. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watkins (U.S. Patent 5,598,517), Rentschler et al. (U.S. 5,821,950) and further in view of Yamaguchi et al. (U.S. 6,040,844).

In reference to claim 13, Watkins and Rentschler et al. disclose all of the claim limitations as applied to claim 12 above however, neither Watkins nor Rentschler et al. explicitly disclose the plurality of texture portions as texels. Yamaguchi et al. discloses a method and apparatus for mapping texture data of three-dimensional computer graphics (see column 1, lines

1-13). Yamaguchi et al. discloses processing texture data in parallel using multiple texture mapping units coupled to a DDA unit (see column 15, lines 41-44, #101a, 102a and 102b of Figure 5). Yamaguchi et al. further discloses the DDA unit to linearly interpolate color values and texture coordinates for a given pixel of a polygon and pass this data onto each texture mapping unit (see column 6, lines 1-8). Note, the office interprets the interpolated texture coordinate data of Yamaguchi et al. functionally equivalent to texel data since this texture data is representative of drawing pixels which in turn represent a portion of the picture for display. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the interpolation in parallel processing techniques of Yamaguchi et al. with the texture parallel processing techniques of Watkins and blending mode operations on texture data of Rentschler et al. in order to enhance image data processing for picture generation while flexibly mapping texture data at increased speeds and at lower costs (see column 5, lines 4-7 of Yamaguchi et al.).

Double Patenting

10. Claims 1-3, 5 and 7-13 are rejected under the judicially created doctrine of double patenting over claims 1-13 of U.S. Patent No. 6,731,296 B2 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

In reference to claim 1, "A system for processing textures for a graphical image on a display, the graphical image including an object, the object including a plurality of fragments, the system comprising a memory for storing a portion part of a program for processing a plurality of texture portions for the plurality of fragments..." of lines 1-5 of claim 1 are claimed in claim 1 of U.S. Patent No. 6,731,296 B2 (see column 12, lines 57-63, or preamble and 1st indent of claim 1). Lines 6-10 of claim 1, "...a plurality of texture processors coupled with the memory, each of the plurality of texture processors for processing a portion of the plurality of texture portions for a fragment of the plurality of fragments in accordance with the program, the plurality of texture processors capable of processing a second portion of the plurality of texture portions in parallel," are claimed in claim 1 of U.S. Patent No. 6,731,296 B2 (see columns 12-13, lines 65-4).

In reference to claim 2, claim 2 in the current application is identical (word for word) to claim 2 in U.S. Patent No. 6,731,296 B2 (see column 13, lines 14-17 or claim 2).

In reference to claim 3, claim 3 in the current application is identical (word for word) to claim 3 in U.S. Patent No. 6,731,296 B2 (see column 13, lines 18-22 or claim 3).

In reference to claim 5, claim 5 in the current application is identical (word for word) to claim 5 in U.S. Patent No. 6,731,296 B2 (see column 13, lines 28-36 or claim 5).

In reference to claim 7, claim 7 in the current application is identical (word for word) to claim 7 in U.S. Patent No. 6,731,296 B2 (see column 13, lines 46-52 or claim 7).

In reference to claim 8, "A method for processing textures of a graphical image on a display, the graphical image including an object, the object including a plurality of fragments, the method comprising the steps of: (a) providing a plurality of texture portions for the plurality

of fragments to a plurality of texture processors, the plurality of texture processors for processing a portion of the plurality of texture portions in parallel..." of lines 1-6 of claim 8 are claimed in claim 8 of U.S. Patent No. 6,731,296 B2 (see columns 13-14, lines 55-7). Lines 7-8 of claim 8, "...processing the plurality of texture portions in the plurality of texture processors based on at least one program," are claimed in claim 8 of U.S. Patent No. 6,731,296 B2 (see column 14, lines 8-10).

In reference to claim 9, claim 9 in the current application is identical (word for word) to claim 9 in U.S. Patent No. 6,731,296 B2 (see column 14, lines 22-26 or claim 9).

In reference to claim 10, claim 10 in the current application is identical (word for word) to claim 10 in U.S. Patent No. 6,731,296 B2 (see column 14, lines 27-31 or claim 10).

In reference to claim 11, claim 11 in the current application is identical (word for word) to claim 11 in U.S. Patent No. 6,731,296 B2 (see column 14, lines 32-36 or claim 11).

In reference to claim 12, claim 12 in the current application is identical (word for word) to claim 12 in U.S. Patent No. 6,731,296 B2 (see column 14, lines 37-41 or claim 12).

In reference to claim 13, claim 13 in the current application is identical (word for word) to claim 13 in U.S. Patent No. 6,731,296 B2 (see column 14, lines 42-45 or claim 13).

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

Allowable Subject Matter

11. Claims 5 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reference to claim 5, the prior art of record (Watkins (U.S. Patent 5,598,517), Rentschler et al. (U.S. 5,821,950), Yamaguchi et al. (U.S. 6,040,844)) does not explicitly disclose a selection means coupled with a bitwise logic, a multiplier-adder, and a summer for selecting a resultant from the bitwise logic, the multiplier-adder and the summer, in combination with the further limitations of claim 5.

In reference to claim 11, the prior art of record (Watkins (U.S. Patent 5,598,517), Rentschler et al. (U.S. 5,821,950), Yamaguchi et al. (U.S. 6,040,844)) does not explicitly disclose the fragment including a program identification and fetching a portion of the program using the program identification.

References Cited

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Dignam (U.S. Patent 6,452,603 B1)

- Dignam discloses a circuit and process performing trilinear filtering using texel data whereby the filtering circuitry includes bit-wise logic, multiplier-adder and summing components.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached at (571) 272-7778.

Any response to this action should be mailed to:

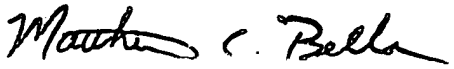
Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.



MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

aac

4/19/05